CLAIMS

I claim:

1. A digital phase-locked tracking loop timing recovery circuit comprising:

an edge detector for detecting an edge transition in an input bit stream;

a digitally implemented loop counter including a plurality of registers indicative of a transition state of said loop counter; and,

a digitally implemented phase counter including a plurality of registers indicative of a transition state of said phase counter, said transition state of said phase counter responsive to detection of said edge transition in said input bit stream, said transition state of said loop counter, and a prior transition state of said phase counter; said transition state of said loop counter responsive to said detection of said edge transition in said input bit stream, a prior transition state of said loop counter and a transition state of said phase counter at said detection of said edge transition.

2. The recovery circuit of claim 1 wherein said circuit generates clock pulses recovered from a stream of input bits.

3. The recovery circuit of claim 2 wherein said transition states of said phase counter are non-linear and include a first set of states indicative of an early phase, and a second set of states indicative of a late phase.

4. The recovery circuit of claim 3 wherein said loop counter can be in one of a plurality of progressively advancing early phase transition states, a plurality of progressively advancing late phase transition states and a neutral state.

5. The recovery circuit of claim 4 wherein said transition state of said loop counter advances toward a maximum early phase transition state when

an edge transition detection occurs during an early phase transition state of said phase counter.

6. The recovery circuit of claim 4 wherein said transition state of said loop counter advances toward said neutral state from a maximum early phase transition state of said loop counter when an edge transition detection occurs during an early phase transition state of said phase counter.

7. The recovery circuit of claim 4 wherein said transition state of said loop counter advances toward a maximum late phase transition state when an edge transition detection occurs during a late phase transition state of said phase counter.

8. The recovery circuit of claim 4 wherein said transition state of said loop counter advances toward said neutral state from a maximum late phase transition state of said loop counter when an edge transition detection occurs during a late phase transition state of said phase counter.

9. The recovery circuit of claim 4 wherein said transition state of said loop counter advances toward said neutral state when an edge transition detection occurs during a punctual transition state of said phase counter.

10. The recovery circuit of claim 4 wherein said transition state of said phase counter advances a set number of transition states when an edge transition detection occurs during an early phase transition state of said phase counter and said loop counter is at a maximum early phase transition state.

11. The recovery circuit of claim 10 wherein said set number of transition states is two transitions states.

12. The recovery circuit of claim 4 wherein said transition state of said phase counter retards a set number of transition states when an edge transition detection occurs during a late phase transition state of said phase counter and said loop filter is at a maximum late phase transition state.

13. The recovery circuit of claim 12 wherein said set number of transition states is one transition state.

14. The recovery circuit of claim 1 wherein said circuit is part of a programmable logic chip.

15. The recovery circuit of claim 1 wherein said circuit is part of an integrated circuit.

16. An integrated circuit for recovering a clock pulse from a stream of input bits comprising:

a digitally implemented phase counter for indicating a phase state of a detected edge of an input bit and enabling a clock output;

a digitally implemented loop counter responsive to said phase state of said phase counter, said phase counter having a transition state responsive to a transition state of said loop counter.

17. The integrated circuit of claim 16 wherein said phase counter includes a plurality of registers for indicating said transition state of said phase counter.

18. The integrated circuit of claim 16 wherein said loop counter includes a plurality of registers for indicating said transition state of said loop counter.

19. The integrated circuit of claim 16 including a register for indicating detection of an edge of an input bit.

20. The integrated circuit of claim 16 wherein said phase states for said phase counter are non-linear.